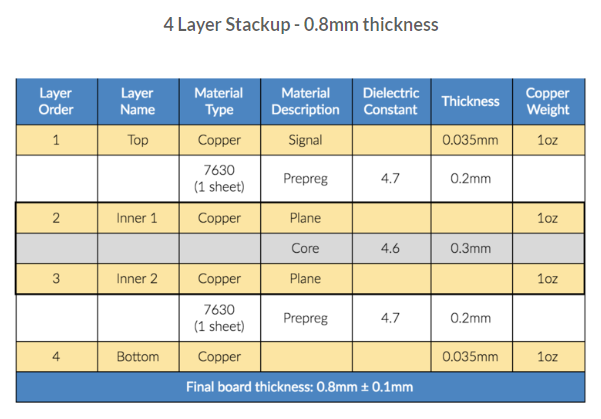
**Layout Rules and Guidelines**

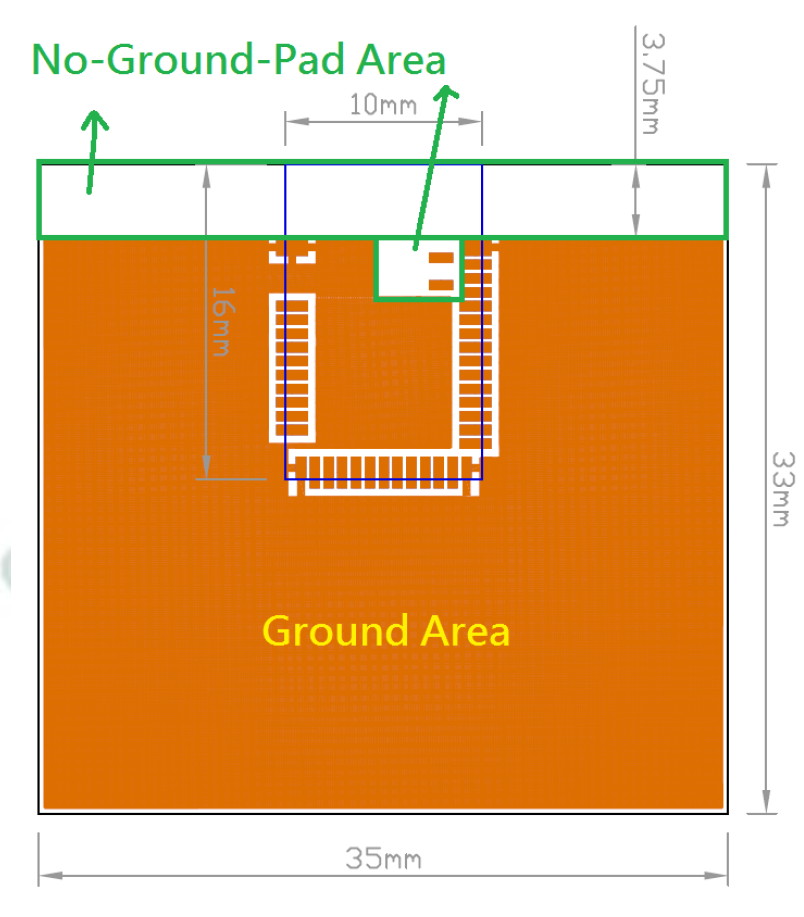
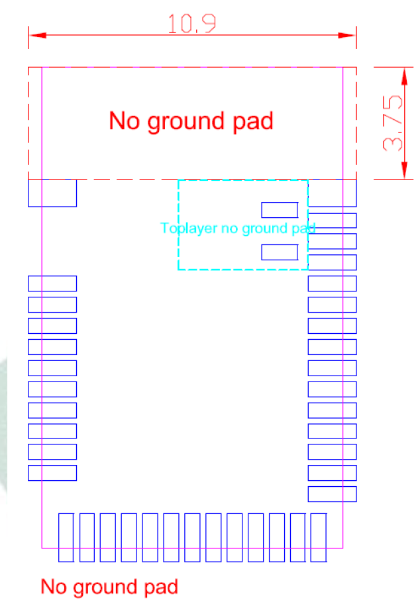
* **General**
  + Use 45 degree bends on all traces.
  + Locate discrete components close to their respective ICs as shown in the schematic diagram unless addressed specifically in this document.
* **Stackup**
  + Thickness: **0.8mm**
  + Material: **FR-4 or equivalent**
  + 4 layers
    - L1 - Signal
      * Thickness: 1oz + Plating
      * Impedances (±10%)
        + Single-Ended: 50Ω
        + Differential: 90Ω
    - L2 - GND
      * Thickness: 1oz
    - L3 - PWR
      * Thickness: 1oz
    - L4 - Signal
      * Thickness: 1oz + Plating
      * Impedances (±10%)
        + Single-Ended 50Ω
        + Differential: 90Ω
  + Details:



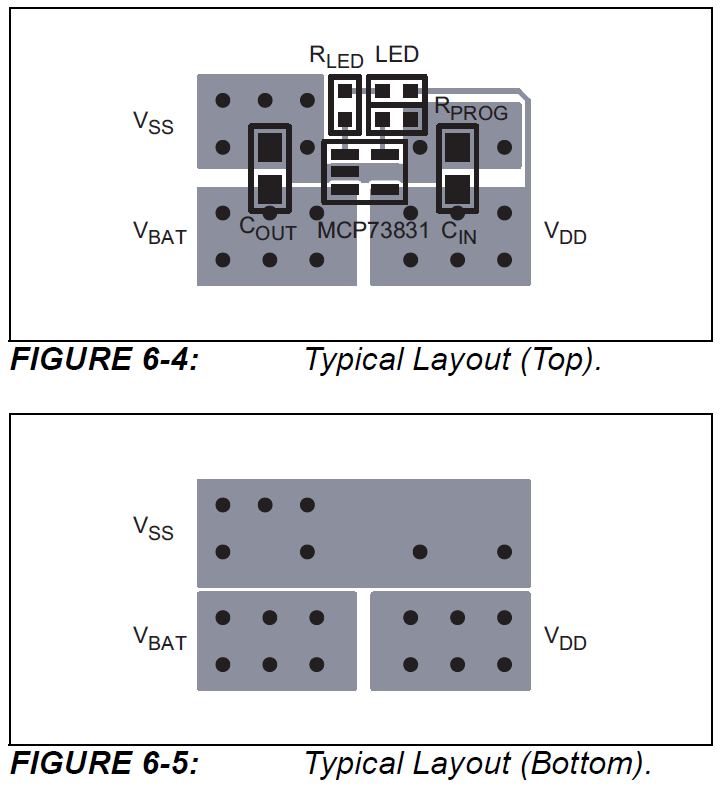
* **Routing Rules**
  + Power (assumes 1oz copper)
    - High Power: 15mil minimum width
      * Signals: 3V3, GND, VBAT, VBUS, VIN\_LDO
    - All Others: 5mil minimum width
  + SWD
    - Signals: SWCLK, SWDIO, SWO
    - Impedance: 50Ω ± 10% single-ended
    - Routing Layers: Layers 1, and 4
    - Maximum trace length of 4 inches.
    - Route signals so that there are no stubs.
    - Keep traces at least 3H away from other signals.
  + USB
    - Signals: USB\_P/N, USB\_IN\_P/N
    - Impedance: 90Ω ± 10% differential
    - Routing Layers: Layers 1 and 4
    - Trace lengths should be matched within 150mil between pairs
    - Route signals so that there are no stubs.
    - A maximum of 1 via may be used along the full trace length.
    - Ground stitching vias should be placed within 50mil of signal transitions from Layer 1 to Layer 4.
    - Traces should not be routed under or between pins of other devices
    - Traces and vias should be kept at least 3H away from other signals/fills.
  + General
    - Do not split signal ground planes.
    - Do not route signals over splits in reference planes.
    - Fill unused PCB areas with GND fills/planes.
    - Add ground-stitching vias every 250mil in ground planes and fills; Stitch the edge of ground planes with vias.
    - Route traces on adjacent layers perpendicular to each other to reduce crosstalk.
    - Keep all clock lines as short as possible.
    - Do not share power and ground pads or use long, narrow traces for decoupling capacitors.
    - Make traces to power supply filtering components as short and wide as possible; vias should be used instead of long, narrow traces to connect to power planes.
    - Use dogbones instead of via-in-pad.
* **Placement Guidelines**
  + In general, ESD diodes should be placed closest to their associated connector, before any other components on the same signal (i.e. capacitors, inductors, etc).
  + Place J1-J3, S1, U2-U3 and U5 on the top and bottom layers in the general areas shown in the figure below.



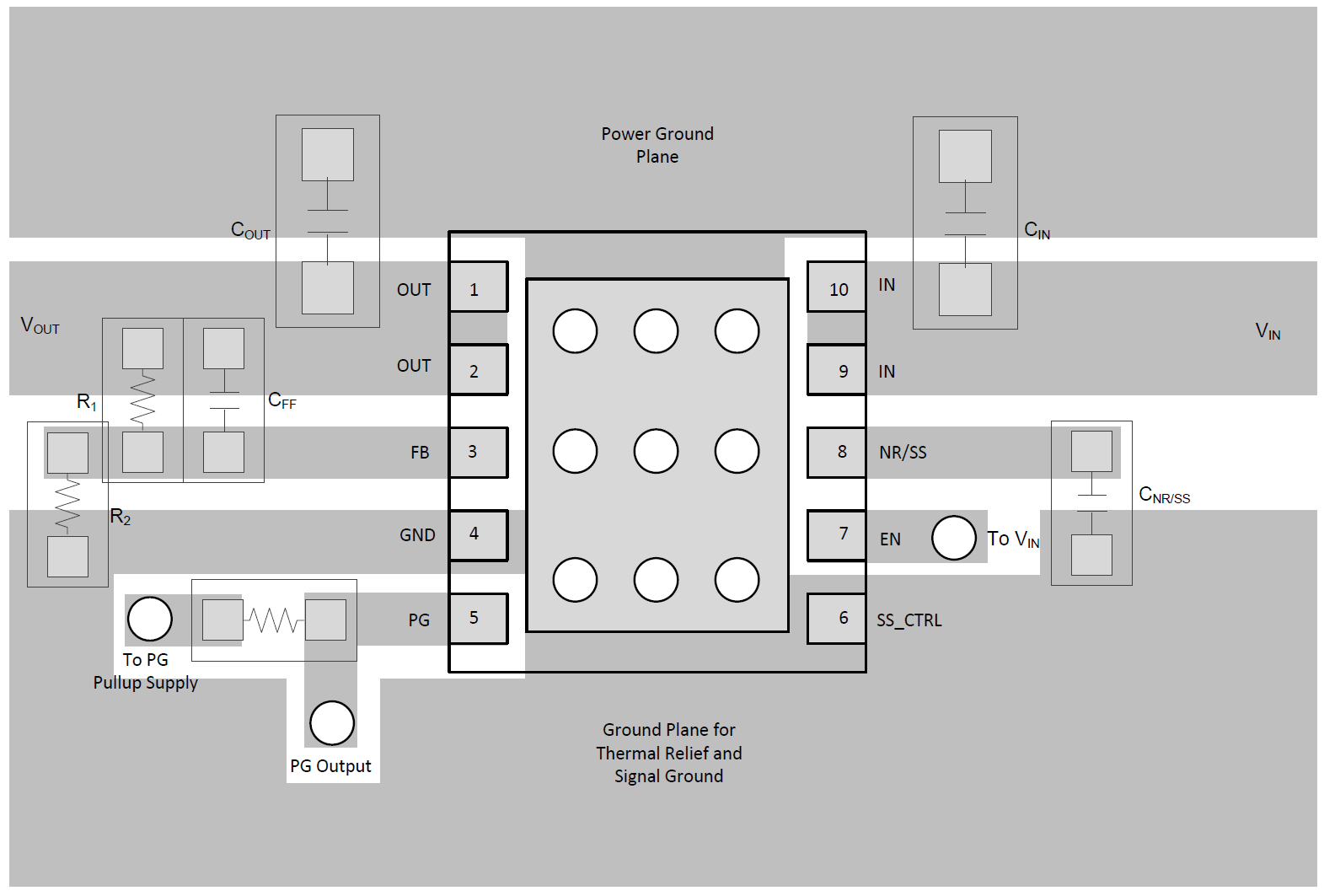
* + Place D1, R1-R2 and U2 near their pins on J1.
  + Place C1, C7, D3, J2, R4, R7-R9 and R11 near their pins on U2.
  + Place C8 and R12 near R11 and D3.
  + Remove GND on all layers and GND on the top layer under U2 in the red and blue areas, respectively, shown in the figures below.



* + Place C2-C3, D2, J3, and R5-R6 near U3.
  + Place battery pack as close to U3 / J3 as possible.
  + Add many vias to conduct heat away from U3 as shown in figures below.



* + Place C4-C6, C9 and R10 near U4.
  + Place C10-C13, D4, Q1, R13-R14 and R17 near U5.
  + Use the layout example in the figure below for U5.



* **Mechanical**
  + Please see the PcbDoc of the MCO for dimensions and hole sizes.
  + Board Thickness: **0.8mm**
  + Height restrictions
    - Top Layer: **9mm**
    - Bottom Layer: **8mm**
* **Manufacturing**
  + Please add the fab number (**BS-V1**) in copper on either the top or bottom layer in a corner of the board.
  + Please add the assembly number (**BS-V1-ASSY**) in silkscreen on either the top or bottom layer in a corner of the board.
  + Create a silkscreen rectangle for writing in the board number in marker.
  + Add MSX Consulting signature in silkscreen on the board.